

FIG. 1

127/114

PROCESSOR BUS 110/
PROCESSOR CORE 112

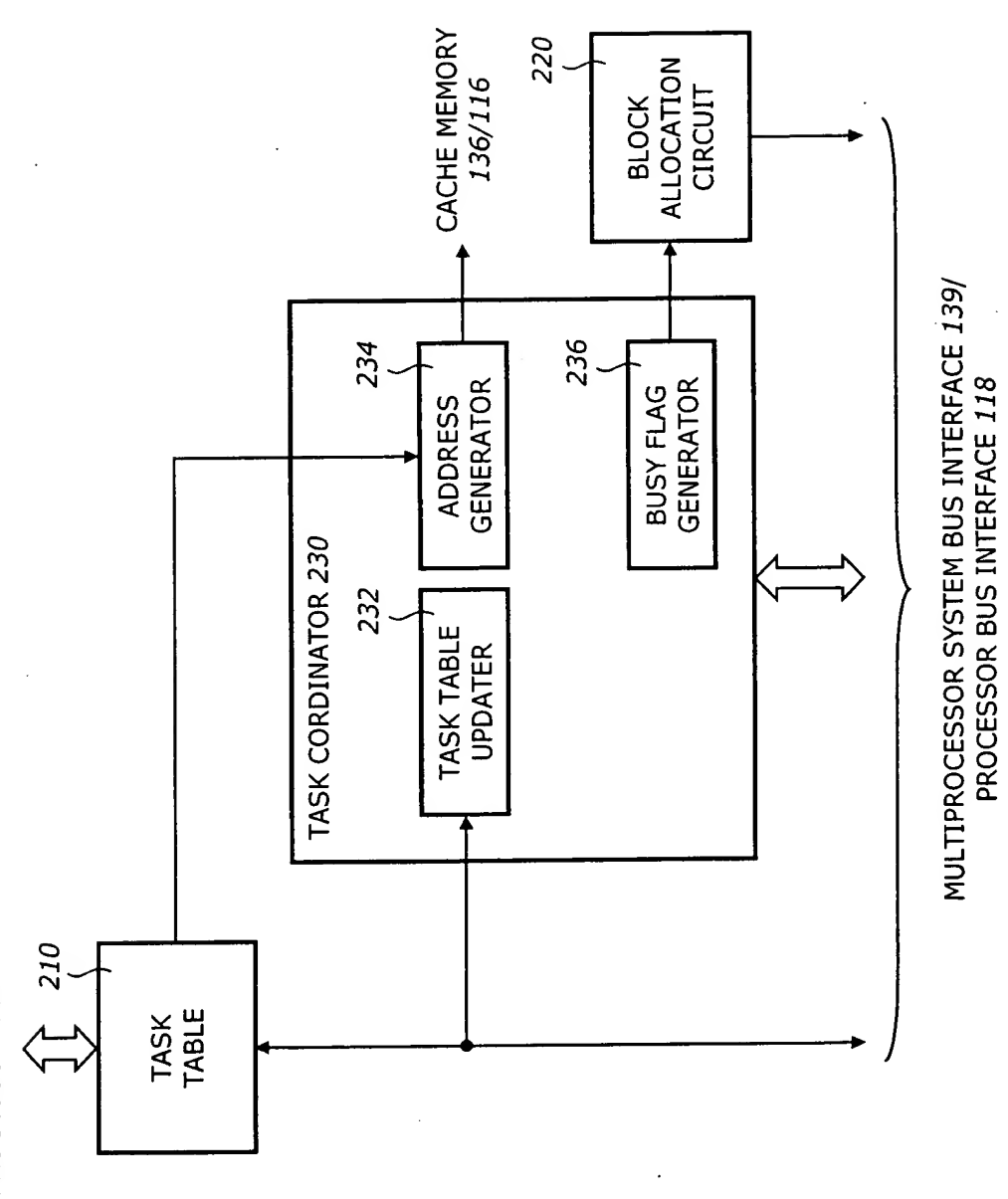
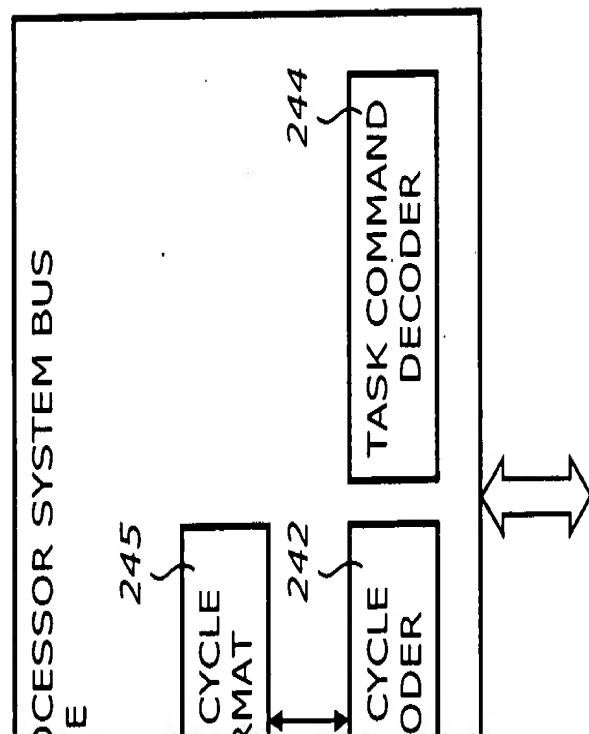


FIG. 2A

139



SYSTEM BUS 140

FIG. 2B

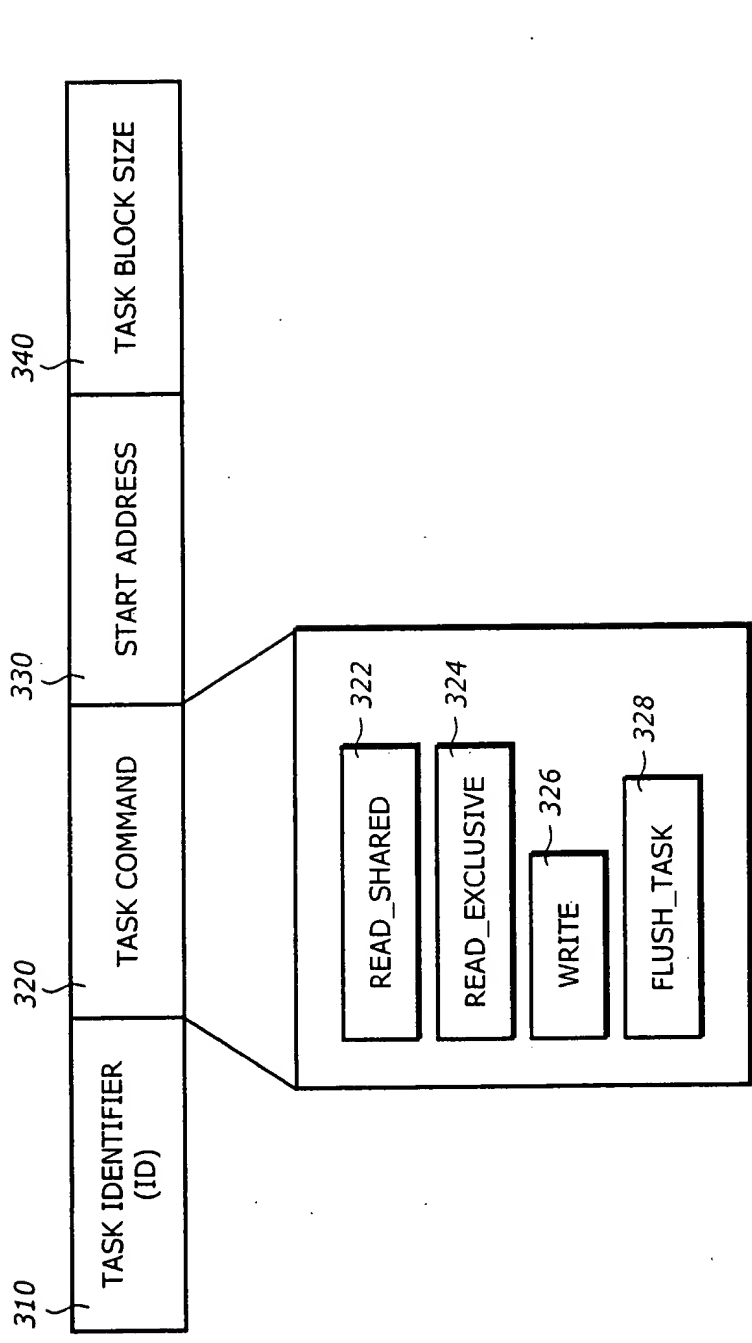


FIG. 3

210

420	430	440	450	460
STATUS	TASK ID	START ADDRESS	TASK BLOCK SIZE	CACHE ADDRESS
INVALID	X	X	X	X
SHARED	00100	0100 0000	0000 1000	000100
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
EXCLUSIVE	00080	0040 0000	0000 0100	006800

410₁

410₂

410_L

FIG. 4

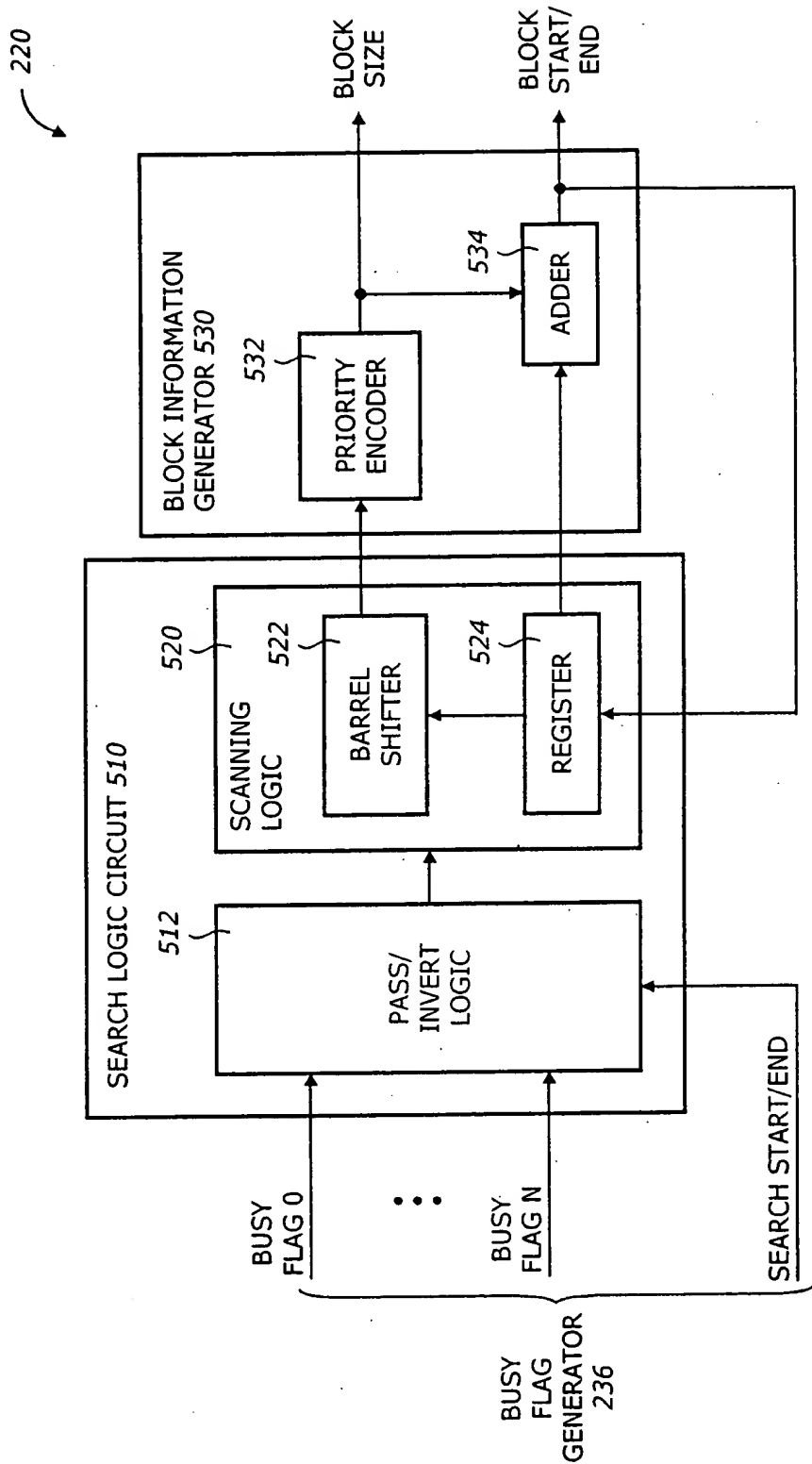


FIG. 5